R&D STATUS REPORT

ARPA ORDER NO. 3771 Amend. No. 1

CONTRACTOR: Caltech

CONTRACT NUMBER: N00014-79-C-0924, ARPA Order-3771

EFFECTIVE DATE OF CONTRACT: September 1, 1979

EXPIRATION DATE OF CONTRACT: February 28, 1982

PRINCIPAL INVESTIGATOR: Carver Mead

TELEPHONE NUMBER: (213) 356-6811

SHORT TITLE: Demonstration of the Use of VLSI Design Rules, Standards, and Interfaces

REPORTING PERIOD: June 1, 1981 to September 1, 1981

Research and development status rept. 1 Jun. - 1 Sep 81

1 Sep 81

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DESCRIPTION OF PROGRESS

Progress is reported for each element of Tasks 1, 2 and 3.

TASK 1

1. Consultation from Fabrication Lines

Work completed; no further progress to report.

2. CMOS-SOS and NMOS-Si Gate Test-Chips

The revised NMOS test-chips have been received. Work is underway to generate the software necessary for the electrical tests.

3. Geometrical Design Rules

A set of CMOS-bulk design rules has been completed.

4. Speed and Timing Rules

The Washington University contract has been extended at no additional cost to allow the CMOS-SOS designs to be evaluated for performance related to speed and timing considerations. Results will appear in the final report.

5. CIF

Modifications to the currently used design program's "ART" and "CART" are underway. These programs consist of PASCAL procedures in which are embedded the CIF primitives that greatly simplify the design effort. The current work consists of specifying test-chip components by PASCAL functions and passing such things as channel width, channel length, lambda, etc. as parameters. In addition, some features such as the 2x10 pad array would remain constant regardless of the change in lambda.

6. Testability Rules

Work is proceeding - see last quarterly report.

TASK 2

1. Design-Rule Checker

Deleted (see quarterly report for December 1, 1979 to March 1, 1980.)

2. CIF/APPLICON, CALMA Conversion Software

The CIF to APPLICON software development has been completed.

3. Circuit Design

Work completed; no progress to report.

TASK 3

1. Contract Negotiations

Contract negotiations have been completed.

2. Fabrication

In early July JPL was informed by ISI that their current software was unable to handle the CMOS-SOS designs. As a result, JPL began developing the necessary software to convert the design files to a MEBES format. The problem was complicated by the fact that four different layer conventions existed; 1) the contractor's CALMA format for critical dimensions and their test structures with eight explicit layers, 2) JPL test-chip designs with seven explicit layers, 3) JPL circuit designs with six explicit layers, 4) CIT designs with six explicit layers but differing from (3).

By September 1, work was completed on the required software to transform all four types of design files to MEBES format, and tapes were mailed to SYNMOS to generate one test plate with all four design file types and each of the required layers.

CHANGES IN KEY PERSONNEL: none

SUMMARY OF SUBSTANTIVE INFORMATION DERIVED FROM SPECIAL EVENTS: none

PROBLEMS ENCOUNTERED OR ANTICIPATED: none

ACTION REQUIRED BY THE GOVERNMENT:

A request for a six month extension, at no additional cost, was submitted to ONR and approved. No further action is required.

FISCAL STATUS:

1.	Amount currently on contract:		$630,718
2.	Expenditures and commitments to date:		
	Campus Salaries and Contracts:	79,991	
	JPL Salaries and Contracts:	495,863	
			$567,854
3.	Funds required to complete all Tasks:		$62,864

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